



Docket No.: 50090-265

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re Application of

Kiyotoshi UEDA, et al.

Serial No.: 09/766,845

Filed: January 23, 2001

Group Art Unit: 2829

Examiner: P. Patel

For: METHOD AND APPARATUS FOR TESTING SEMICONDUCTOR INTEGRATED CIRCUIT, AND SEMICONDUCTOR INTEGRATED CIRCUIT MANUFACTURED THEREBY

THE COMMISSIONER FOR PATENTS AND TRADEMARKS  
Washington, DC 20231

Dear Sir:

Transmitted herewith is an Amendment in the above identified application.



No additional fee is required.



Applicant is entitled to small entity status under 37 CFR 1.27



Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	14	20	0	\$18.00 =	\$0.00
Independent Claims	2	3	0	\$84.00 =	\$0.00
Multiple claims newly presented					\$0.00
Fee for extension of time					\$0.00
Total of Above Calculations					\$0.00



Please charge my Deposit Account No. 500417 in the amount of \$0.00. An additional copy of this transmittal sheet is submitted herewith.



The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

David M. Tennant

Registration No. 48,362

600 13<sup>th</sup> Street, N.W.  
Washington, DC 20005-3096  
(202) 756-8000 SAB:DT:vgp  
Facsimile: (202) 756-8087  
Date: October 8, 2002

PATENT

RECEIVED

OCT-9 2002

TECHNOLOGY CENTER 2800